identifier having the value b*cxZ, where b and c are as defined above and where Z is the number of elements in each Z-vector and where x represent a multiplication operation.

Please replace the paragraph beginning at page 12, line 14, with the following rewritten paragraph:

At the receiver side, the direct mapping between data bits and transmission units is conformed for demodulation. We assume that soft-outputs from the decoder have the same ordering as the binary code word structure, e.g., as shown in array 600. The soft values includes, however, K bits corresponding to a coded bit. Each of * K bits may be stored in a different one of D arrays where D is a positive integer. In most cases, * K is an integer multiple of D. An exemplary memory 700 has three-bit soft values for each bit, each identified by the same code bit identifier. Those three bits might be in one memory location; or those three bits are in three different memory location 701, 702, 703, as shown in 700. With this structure, it is clear that the same interleaving circuit 600 can be used to access soft values for a transmission unit for demodulation.

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Please replace the paragraph beginning at page 13, line ~~21~~, with the following rewritten paragraph:

~~Many of the~~ The above described method ~~methods or~~ and method steps can be implemented using machine executable instructions, such as software, included in a machine readable medium such as a memory device, e.g., RAM, floppy disk, etc.

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is clear that the same type of interleaving apparatus used in a transmitter can also be used in a receiver to access soft values corresponding to a transmission unit for purposes of demodulation.

Please replace the paragraph beginning at page 10, line 30, with the following rewritten paragraph:

~~Coded bits are stored in memory configured as Z x n. Or equivalently, we view the binary codeword as n Z-vectors, each vector including Z bits. The Z used in vector LDPC codes is a multiple of P, the number of bits associated with a transmitted symbol. For assumed QPSK modulation where P=2, we have Z=2z. We further select the number of columns to be a multiple of M, the number of information transmission symbols in a transmission unit, i.e. n=aM.~~ An interleaving method of the invention determines the location of the 2 bits associated with each symbol in each transmission unit. Clearly, the memory location corresponds to a Z-vector identifier and the ~~offset value~~ bit index inside the Z-vector. The present invention orders coded data as follows: The jth dwell (where j is from ~~0~~ 0 to z x a-1) will contain 2bits *in the Z* ~~bits~~ *vector identified by* ~~i = a/M + (j-(Z/P)] [j/s] + a * i~~ *with* bit index ~~offset value~~ *2* (j mod Z/P)*, where i is from 0 to M-1. In such a case, the address used to retrieve the data bits can be easily generated algebraically, without the use of memory for this purpose.

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Please replace the paragraph beginning at page 11, line 5, with the following rewritten paragraph: